Amendments to the Drawings

Please replace the sheets containing Figures 1 to 5 and 8 with the revised sheets enclosed herewith. In the amended drawings, descriptive text labels have been added to rectangular boxes which previously did not have such labels. The drawings are otherwise not amended.

REMARKS

Drawings

As requested by the Examiner, the drawings are amended to show descriptive text labels for rectangular boxes which were previously shown without text labels.

The Examiner objected to the drawings as not showing every feature specified in the claims. The Applicant respectfully traverses this objection with the following submissions:

- The feature "wherein calculating the drift rate comprises calculating a first order time derivative" (claim 4) is shown in block **120** (Figure 6), labeled as "DETERMINE DRIFT FROM PREVIOUS OFFSET AND TIME SINCE PREVIOUS OFFSET DETERMINED".
- The feature "wherein one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on timing information of the first bus" (claim 6) is shown in the block diagram in Figure 5. A processing element, shown as block **52**, applies a rule to determine when device **14** on bus **18** is to begin an operational cycle. The processing element controls an adjustable delay, shown as block **58**, to alter a length of one or more operational cycles of device **14** (see paragraphs 27 – 29 of the specification).
- The feature "cameras adjust their timing by selectively reading an adjustable amount of extra data for each frame" (claim 9) is shown as the step at block **214** (Figure 7), labeled as "ADJUST LENGTH OF FRAME TO IMPROVE SYNCHRONIZATION". The frame length is the time the camera takes to complete a current frame. The frame length can be extended by reading more unnecessary data, and the frame length can be reduced by reading less unnecessary data (see paragraphs 33 – 34 of the specification).

- The feature "automatically broadcasting timing information on the first and second buses" is not found in the pending claims. It is presumed by the Applicant that the Examiner was referring to the broadcasting of a timing offset to a device on a bus, as recited by claims 19 and 22. Claim 19 recites "broadcasting the first timing offset to the one or more devices on the first bus and the second timing offset to the one or more devices on the second bus..." Claim 22 recites "program memory containing software instructions programmed to cause processing element to calculate a timing offset between the first bus and the second bus and broadcast the timing offset to the one or more devices on the second bus by means of the second interface". It is submitted that these features are shown as the step at block **122** (Figure 6), labeled as "WRITE DRIFT AND OFFSET INFORMATION TO DEVICE(S) ON SLAVE BUSES". Paragraph 25 of the specification discloses that block **122** illustrates that the most recently determined timing offset and drift rate are broadcast to devices **14** on slave bus **18**.
- The applicant submits that the feature "a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses" (claim 25) is not amenable to depiction in the drawings. In any event, the claimed devices are shown in the drawings.

Compliance with 35 U.S.C. §101 (Claims 2 and 18)

Claims 2 and 18 have been amended to clarify that the time measurement for the second bus is taken midway between the first and second time measurements for the first bus. It is submitted that this amendment adds no new subject matter. A person of skill in the art would understand that the method of averaging timing offsets between the first and second buses over a

number of time measurements, as claimed in claims 2 and 18 and described in the specification at paragraph 16, implicitly requires these time measurements to be performed at equally spaced-apart intervals. Indeed, the Examiner noted this point.

Compliance with 35 U.S.C. §112 (Claim 12)

The Examiner rejected claim 12 on the basis that it does not identify the particular version of IEEE 1394 with which the first and second buses are compatible. The Applicant submits that claim 12 is satisfied by compliance with any IEEE 1394 standard. IEEE 1394 is currently defined in the documents for IEEE 1394-1995 (the original version) and IEEE 1394a-2000 and 1394b-2002 (the amendments). It is submitted that a person of skill in the art would readily be able to determine whether or not any particular bus is or is not compliant with a version of IEEE 1394 and that claim 12 satisfies the requirements of 35 U.S.C. §112.

Compliance with 35 U.S.C. §102 and §103

The Office Action alleges that all of the features in the pending independent claims are disclosed by U.S. Patent No. 4,807,259 (Yamanaka *et al.*). The Applicant submits that this is incorrect.

As understood, Yamanaka *et al.* disclose sending encoded timing signals between a master station and a slave station in order to synchronize the time of a slave clock in the slave station with the time of a master clock in the master station. The master station and slave stations each have an internal bus. The master station exerts centralized control over a data link between the master and slave station (see col. 1, ln. 41-43) and synchronizes the slave clocks with the master clock by exchanging messages with the slave stations. Synchronization is performed separately for each slave station. The slave station uses the slave clock time directly.

Claims 1 to 17

The Applicant points out that claim 1 recites four entities that maintain timing, namely, the first and second buses, one or more devices on the first bus, and one or more devices on the second bus.

The Applicant understands that the Examiner has equated the first and second buses claimed in claim 1 with the buses (51, 52) in the master and slave stations, and the timing information from the first bus and the second bus in claim 1 with the times (TM, TS) maintained by the master and slave clocks (17, 27). The Applicant submits that master clock (17) and slave clock (27) appear to operate independently of the buses (51, 52) to which they are connected and therefore, they cannot be said to be timing information of those buses. In any event, Yamanaka fails to disclose any devices on the first or second buses that maintain timing information independently of master clock (17) or slave clock (27). The time **TS** of Yamanaka's slave clock (27) cannot be both timing information of the second bus and timing of a device on the second bus.

Further, Yamanaka fails to disclose "broadcasting the timing offset to the one or more devices on the second bus so that the one or more devices on the second bus can adjust their timing to be synchronized with the one or more devices on the first bus" as recited in claim 1. This is not necessary in the Yamanaka system because the slave clock (27) is kept synchronized with the master clock (17) to a desired degree of accuracy.

The Applicant points out that Yamanaka separately synchronizes each slave clock (27, 37) by separately exchanging messages between the master station and the slave station in which the slave clock is located. In the invention claimed in claim 1 of this application, one or more devices on a second bus can synchronize their operations with devices on a first bus by receiving

a broadcast timing offset between the first and second buses. It is not necessary for any master station to communicate individually with the devices to perform the synchronization.

Therefore, it is submitted that independent claim 1 patentably distinguishes Yamanaka *et al.*

The Applicant respectfully requests rejoinder of claims 5, 8, 10, 11 and 13 on the basis that allowable claim 1 is generic to all of claims 2 to 17. The Applicant submits that dependent claims 2 to17, which all depend from claim 1, are patentable over Yamanaka *et al.* at least because they depend from claim 1.

Claim 18

Independent claim 18, as amended, recites "a method of synchronizing one or more devices on a first bus with one or more devices on a second bus, the method comprising: (a) taking a first time measurement for the first bus; (b) taking a time measurement for the second bus; (c) taking a second time measurement for the first bus, wherein the time measurement for the second bus is taken midway between the first and second time measurements for the first bus; (d) calculating an average of the first and second time measurements for the first bus; (e) subtracting the time measurement for the second bus from the average to determine a timing offset between the first bus and the second bus..." Claim 18 further recites that a drift rate is to be calculated based on the difference between the stored timing offsets. The Applicant submits that Yamanaka *et al.* do not disclose a method comprising taking time measurements for a first bus and a second bus and calculating an average of the time measurements for the first bus. Yamanaka *et al.* also do not disclose the calculation of a drift rate based on a difference between the stored timing offsets.

Further, claim 18 recites "adjusting timing of the one or more devices on the second bus to be synchronized with the one or more devices on the first bus based on the broadcast timing offset and a time of the second bus". As noted above in relation to claim 1, Yamanaka et al. do not disclose setting a time associated with any device based upon a time of a second bus and an offset. Yamanaka periodically corrects the time of slave clocks (27, 37) and subsequently uses the times maintained by the slave clocks to record the times that various events occur. Any devices that have access to slave clock (27 or 37) can treat the slave clock as being accurate since it is synchronized to the master clock (17) periodically. Such devices do not need to deal with any offset. Given these distinctions, the Applicant submits that claim 18, as amended, is patentable over Yamanaka.

Claims 19 to21

The Applicant points out that independent claim 19 recites at least five entities that maintain timing, namely, the first, second and master buses, one or more devices on the first bus, and one or more devices on the second bus.

The Office Action asserts the following correspondence between features of Yamanaka and the claimed invention:

Yamanaka	Claim 19
bus (51)	master bus
bus (52)	first bus
bus (53)	second bus
TM	time of master bus
TS (of slave clock (27))	time of first bus
TS (of slave clock (37))	time of second bus

The Applicant points out that Yamanaka fails to disclose any devices to which offset information is broadcast. Claim 19 recites "broadcasting the first timing offset to the one or more devices on the first bus and the second timing offset to the one or more devices on the second bus so that the one or more devices on the first bus and the one or more devices on the second bus all begin their respective operational cycles at the same global time".

By contrast, Yamanaka transmits a time difference (T_{D1}) between master clock (17) and slave clock (27), to slave station (2). CPU (20) of slave station (2) then corrects the setting of slave clock (27) (see col. 7, ln. 42-45). Subsequently, slave station (2) uses slave clock (27). Time difference (T_{D1}) is not a timing offset between two buses, nor is it broadcast to devices on the buses so that the devices can begin their respective operational cycles at the same global time.

Claims 22 to 29

Independent claim 22 recites "a processing element coupled to the first and second buses by the first and second interfaces respectively" and software instructions that cause the processing element to broadcast a timing offset to one or more devices on the second bus. These features are not disclosed by Yamanaka. In the Yamanaka system, processing element (10) appears to be connected directly to interface (51) and communicates to slave stations (2,3) also by way of bus (51) and circuits (19, 18).

In relation to claim 25, the Examiner has overlooked the fact that the claim compares the sum of bandwidths of the devices on the first and second buses to maximum allowable bandwidths of the first and second buses. It is not inherent that the claimed relationship will be satisfied.

In relation to claim 29, Applicant points out that if a person attempted to combine Yamanaka and Yagita then the person would either attempt to treat each camera as a slave station

and synchronize each slave station as described by Yamanaka or provide a slave clock accessible to all of the cameras and keep the slave clock synchronized with a master clock as described by Yamanaka. One would not arrive at the claimed invention which involves broadcasting the timing offset to the plurality of cameras.

Applicant respectfully requests rejoinder of claims 27 and 28 on the basis that allowable claim 22 is generic to all of claims 23 to 29.

The Applicant accordingly submits that claims 22 to 29 are patentable over the cited references.

New Claims

The Applicant submits that new claims 30-32 patentably distinguish the cited references and are supported by the specification as filed.

Conclusion

The Applicant submits that all claims of this application are in condition for allowance. The Applicant respectfully requests reconsideration and allowance of this application.

Respectfully submitted,

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